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GaAs FET LIMITING AMPLIFIER DESIGNED FOR LOW AM TO PM CONVERSION

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A 0.5 μm gate length GaAs FET has been characterized for use in a low AM to PM conversion limiting amplifier at 12.0 GHz. A unique linear behavior for FET AM/PM is observed with respect to DC biasing, and its data are presented along with input and output matching information. FET limiting amplifier design techniques and data on a nine-stage amplifier are also reported.

Introduction

With the advance in performance of GaAs FETs, their use in limiting amplifiers at Ku Band frequencies is becoming practical, rivaling the tunnel diode limiting amplifier. Some work[1,2] has been published describing these devices when used in strongly nonlinear applications and a few[3,4] papers have been published describing GaAs FET Amplifier AM to PM conversion behavior. However, little work has been reported when the gains of the devices have been compressed from a positive value to 0 dB.

This paper reports the testing and data obtained with 0.5 μm and 1.0 μm GaAs FETS. The bias and matching dependence of AM to PM conversion has been investigated and unique linear behavior with respect to different biasing has been observed. As a demonstration, a one stage amplifier has been designed using these data. The approach used in this design is explained and the amplifier performance is predicted. The feasibility of this undertaking has been demonstrated with a nine-stage amplifier built using 0.5 μm and 1.0 μm transistors. The performance of this amplifier is also presented.

Transistor Characterization

It is well known that the AM to PM conversion behavior of a GaAs FET amplifier due to the nonlinear behavior of the devices is a function of the bias and the match presented to the input and output. An active bias scheme has been chosen for the transistor so that the drain-source voltage and drain current are approximately constant over the range of input powers incident on the transistor. This provides a fixed, known operating point across the input power range and helps limit the gain and DC power dissipation at high input power levels by forcing the gate-source voltage more negative.

Since the AM to PM conversion is a function of bias point and input-output match, a means to vary and monitor these parameters simultaneously was desired. The test station used to accomplish this is an augmentation of a load pull measurement technique[5] that adds source pull capability. It is outlined in Figure 1. The loss in the coupler and bias tees limits the range of matches which can be presented to the transistor. For some of the measurements, an active tuner was used on the input to extend this range.

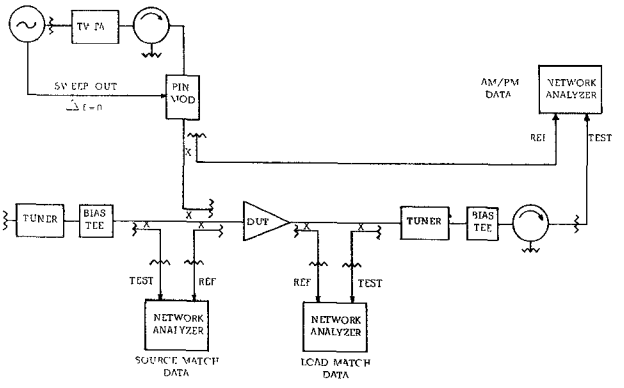

FIGURE 1. Source and Load Pull AM to PM Characterization Testing

Over a wide range of bias points, a pair of input and output matches can be found that yield an amplifier with near zero AM to PM conversion (less than 2°) with the FET severely compressed, i.e., 0 dB gain. With these input and output matching conditions fixed, it has been found that within our measurement accuracy, there exist linear contours in the bias plane (drain current versus drain-source voltage) that leave the AM to PM conversion almost unaltered as shown in Figure 2. Each curve in Figure 2 corresponds to different pairs of matching conditions at the input and output of the transistor. Movement along these contours will, for example, change the small signal gain or saturated output power dramatically but

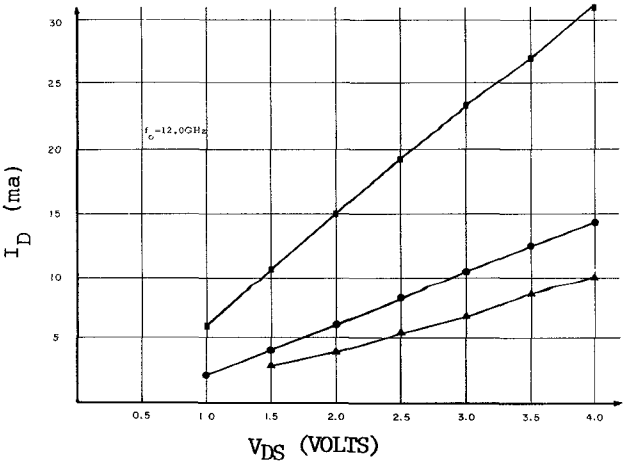

FIGURE 2. 0°/dB Contours in Bias Plane for Constant AM to PM Conversion at Three Different Input and Output Matching Conditions.

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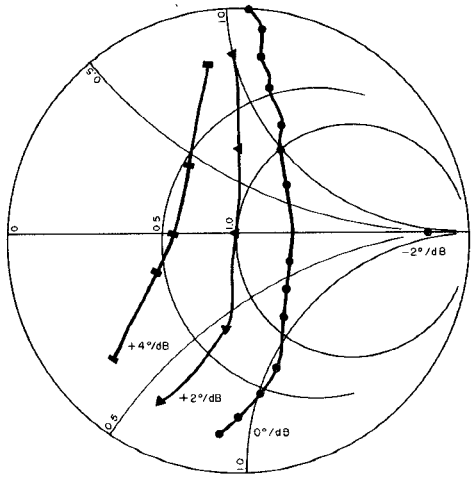
leave the AM to PM unaffected. Bias points lying above the 0°/dB contour for each match condition correspond to a phase shift of constant sign and points below correspond to the opposite sign. Thus, a tool is provided for designing or adjusting a FET limiting amplifier to achieve low AM/PM conversion.

Likewise, if the bias point and either the input or output match are fixed, there exist contours of constant AM to PM conversion in the other matching plane. Typical contours are illustrated in Figures 3 and 4. For some matching conditions there is no 0°/dB contour inside the region of the Smith Chart to which we could match.

The theoretical explanation for this behavior is in-progress along with device nonlinear modeling and computer simulation.

Amplifier Design

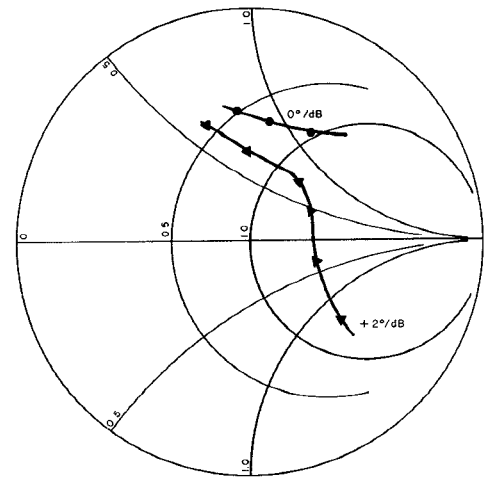
Small signal data was also taken on the 0.5 μm device. This data and the AM to PM conversion data were used to design a single stage limiting amplifier.



f_o = 12.0 GHz Output Match Γ = .50 < 50°
V_{DS} = 4.0V I_D = 14 ma

FIGURE 3. Contours in Input Matching Plate for Constant AM to PM Conversion

As is the case with a low noise design, the input/output matching circuits needed for maximum small signal gain do not correspond to best AM to PM conversion and reasonable gain. Circles of constant gain were plotted in both the input and output plane and matching circuits selected as a compromise between small-signal gain and low AM to PM conversion. Our choice was to sacrifice 1 dB of gain at both the input and output. The small signal data indicated a maximum available gain of 9 dB at 12.0 GHz over 500 MHz bandwidth. Thus, our design is for a 7 dB single stage amplifier with zero AM to PM conversion. Its topology is presented in Figure 5. Single-ended amplifiers will be cascaded using drop-in isolators for interstage coupling and input and output matching.



f_o = 12.0 GHz Input Match Γ = 0
V_{DS} = 4.0V I_D = 14 ma

FIGURE 4. Contours in Output Matching Plane For Constant AM to PM Conversion

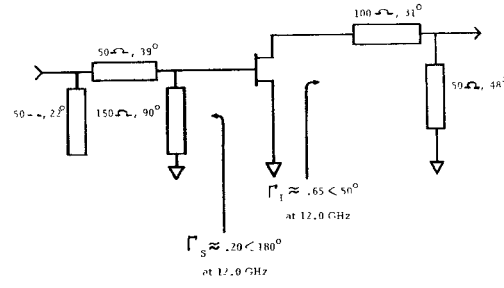


FIGURE 5. Topology and Matching for 12.0 GHz Limiting Amplifier

A Nine-Stage Amplifier

The feasibility of a low AM to PM FET limiting amplifier was demonstrated by the construction of a nine-stage amplifier using both 0.5 μm and 1.0 μm transistors. The stages were previously designed for small signal gain. By properly adjusting DC biasing, each stage could exhibit either positive, negative, or zero AM/PM from small signal gain to 0 dB gain. This 53 dB gain amplifier has a total phase shift of less than 12° from small signal gain to 50 dB into compression as shown in Figure 6.

Summary

A source and load pull method has been used for large signal characterization of 0.5 μm and 1.0 μm FET devices. The 12 GHz data for a 0.5 μm FET has been presented. The unique linear behavior of FET AM/PM conversion in I_{DS} versus V_{DS} bias plane has been reported. The input and output matching data have also been presented. From these test

results, a technique to design low AM/PM limiting amplifiers has been described and its feasibility has been demonstrated with a nine-stage amplifier which exhibits an excellent AM/PM performance of less than 12° total phase shift.

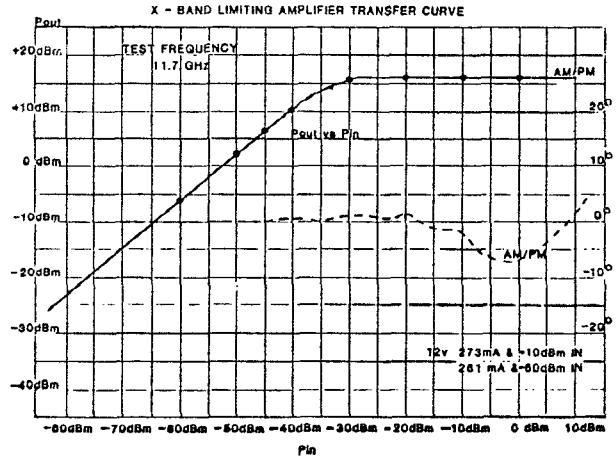


FIGURE 6. AM/PM and Output Power Transfer Curve for Nine-Stage Limiting Amplifier

Acknowledgements

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